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☐ 1. Document ID: US 6665746 B1

L2: Entry 1 of 2

File: USPT

Dec 16, 2003

US-PAT-NO: 6665746

DOCUMENT-IDENTIFIER: US 6665746 B1

TITLE: System and method for prioritized context switching for streaming data memory transfers

DATE-ISSUED: December 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Liong; Thomas S.	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machine Corporation	Armonk	NY			02

APPL-NO: 09/ 540773 [PALM]

DATE FILED: March 31, 2000

INT-CL: [07] G06 F 13/28

US-CL-ISSUED: 710/22; 710/26, 710/40, 709/103, 709/108

US-CL-CURRENT: 710/22; 710/26, 710/40, 718/103, 718/108

FIELD-OF-SEARCH: 710/22-24, 710/26, 710/33, 710/42, 710/48

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>5251303</u>	October 1993	Fogg et al.	710/24
<u>5802546</u>	September 1998	Chisholm et al.	711/100
<u>5894560</u>	April 1999	Carmichael et al.	710/25
<u>6105075</u>	August 2000	Ghaffari	710/5
<u>6105080</u>	August 2000	Holt et al.	710/26
<u>6298403</u>	October 2001	Suri et al.	710/100
<u>6389449</u>	May 2002	Nemirovsky et al.	709/108
<u>6418489</u>	July 2002	Mason et al.	710/22

ART-UNIT: 2182

PRIMARY-EXAMINER: Gaffin; Jeffrey

ASSISTANT-EXAMINER: Sorrell; Eron J.

ATTY-AGENT-FIRM: Dorsey & Whitney LLP

ABSTRACT:

Method of streaming data transfers from scattered locations or to a gathered location in a memory, including the steps of manipulating the transfer of data between memory devices by processing, an element at a time, entries in a first scatter/gather list; upon receipt of a request to process a second scatter/gather list, interrupting the processing of the first list; and resuming the processing of the first list upon the completion of the processing of the second. In one embodiment, the step of interrupting the processing of the first scatter gather list interrupts only at the completion of the processing of an element of the first scatter/gather list and prior to the retrieval of the next element in the first scatter/gather list. In another embodiment, the interrupting step further includes storing the next address to be processed in the first scatter/gather list, and retrieving the first element in the second scatter/gather list. Provides a scatter/gather mechanism for streaming transfers between a first and second memory device without processor or firmware intervention. The mechanism comprises: a transfer engine for streaming data transfers between dispersed locations in one memory to a gathered location in a second memory, means for suspending processing of a current transfer request upon the receipt of a second request, and means for resuming the processing of a suspended transfer request including a pointer for indicating the starting address of a next element to be processed in a suspended transfer operation. Computer program and computer program product are also provided.

22 Claims, 5 Drawing figures

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KWIC	Draw Desc	Image
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☐ 2. Document ID: US 6105080 A

L2: Entry 2 of 2

File: USPT

Aug 15, 2000

US-PAT-NO: 6105080

DOCUMENT-IDENTIFIER: US 6105080 A

TITLE: Host adapter DMA controller with automated host reply capability

DATE-ISSUED: August 15, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Holt; Keith W.	Wichita	KS		
Weber; Bret S.	Wichita	KS		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
LSI Logic Corporation	Milpitas	CA			02

APPL-NO: 09/ 000681 [PALM]

DATE FILED: December 30, 1997

INT-CL: [07] G06 F 13/28

US-CL-ISSUED: 710/26

US-CL-CURRENT: 710/26

FIELD-OF-SEARCH: 710/22, 710/26, 710/126, 710/129

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>5542053</u>	July 1996	Blaud et al.	710/129
<u>5708849</u>	January 1998	Coke et al.	710/22
<u>5864712</u>	January 1999	Carmichael et al.	710/20

ART-UNIT: 271

PRIMARY-EXAMINER: Auve; Glenn A.

ABSTRACT:

A DMA controller operable within a host adapter which automatically transmits replies to an attached host system to thereby reduce overhead processing in the I/O processor of the host adapter. The DMA controller is preferably operable to perform DMA transfers in accordance with one or more scatter/gather lists descriptive of the desired data transfer. A flag bit associated with and/or contained in entries of the scatter/gather list signifies the need to transmit a reply message to the host system. The requisite reply message is transmitted to the host system by the DMA controller following the DMA transfer of the block defined by the scatter/gather list entry containing the indicator. The reply message content is determined in accordance with information associated with and/or contained in the subsequent entry of the scatter/gather list. The subsequent scatter/gather list entry includes a reference to the reply message content and a reference to the destination location to which the reply is transmitted. In the preferred embodiment, the host adapter is operable in accordance with the industry standard I2O specifications. A reply message is transmitted to the I2O compatible host system interface via I2O defined outbound queues and context structures defined in the subsequent scatter/gather list. In addition, the reply message may be either static and predefined or dynamically generated by the DMA controller. Further, the destination for the reply message may be either statically encoded in the scatter/gather list entry or may be dynamically obtained from the context structures by the DMA controller.

18 Claims, 5 Drawing figures

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	Draw Desc	Image
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Term	Documents
"6105080"	1
6105080S	0
(1 OR ("6105080".PN.)).USPT.	2
(L1 OR (6105080.PN.)).USPT.	2